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(54) Information processing apparatus and data back-up/restore system for the information processing apparatus.

(57) An information processing apparatus backs up status of a CPU (10) and content of a main memory (30) into a back-up memory (50) at the time of power-off, restores the data backed up in the back-up memory at the time of power-on to resume data processing, and informs the start of the resumed data processing or the termination of the data processing by a buzzer.

Fig. 1A

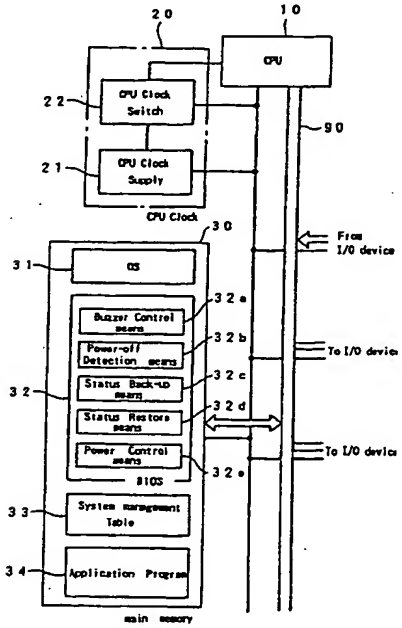
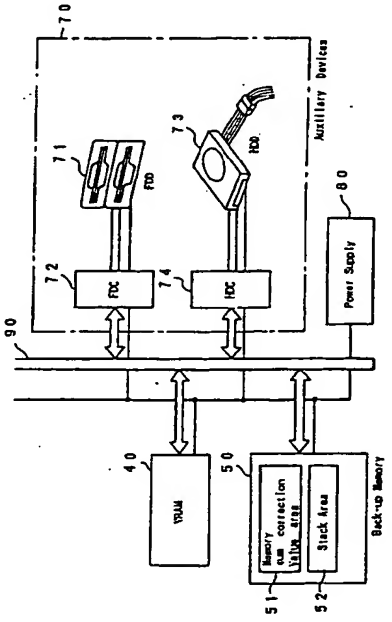


Fig. 1C



EP 0 481 508 A2

Background of the Invention

(Field of the Invention)

The present invention relates to an information processing apparatus having a processor control unit such as a personal computer or a personal word processor.

(Related Background Art)

Some of recent portable or transportable information processing apparatus such as personal computers and personal word processors have an internal data preserve function which preserves a status at the time of power-off and restores the preserved status when the power is next turned on to continue the data processing. In this function, all status at the time of the power-off including the displayed content are stored in a memory when the operation status of the information processing apparatus is displayed on a display screen and when the power is turned on again, the information processing apparatus can resume with the same status as that at the time of the power-off. When such a mechanism is operated, an operator notices the power-off because a brightness of the display or a back light is darkened when a power switch is turned off during the operation of the information processing apparatus. However, in actual, data is being moved to the memory in the information processing apparatus to back up the data. When all processing are completed after a predetermined time period, a portion or all of the power supply circuit are turned off. When the power switch is turned on from the turn-off state, the operator notices it because the display is brightened. However, in the processing unit, the backed-up data is being mov d to the memory of the processing apparatus or the display and the processing apparatus does not work even if the operator depresses a key of a keyboard. That is, the completion of restore of the preserved status delays from the timing of the power-on when such a function is installed, and there is no means to clearly determine when the restore of the preserved status has completed.

Further, the movement of the back-up data to the processing apparatus when the power is turned on may not be normally performed. In such a case, the processing apparatus does not work even if a key of the keyboard is depressed, or even if it works, the xecution gradually becom s out of order.

Summary of the Inv ntion

It is an object of the pres nt inv ntion to provide an information processing apparatus comprising: memory means connected to control means through a bus line; status back-up means for backing up the status of said control means and the content of the memory means at the time of power-off; status restore means for restoring the status backed up in the status back-up means at the time of power-on to resume the data processing; and inform means for informing the termination of the data restoring processing. The inform means of the information processing apparatus detects a time delay between the time of power-on of the apparatus and informs it to a user.

It is another object of the present invention to provide a data back-up/restore system of an information processing apparatus comprising memory means connected to control means through a bus line; status back-up means for backing up the status of said control means and the content of the memory means at the time of power-off; and status restore means for restoring the status backed up by the status back-up means at the time of power-on to resume the data processing; wherein the system comprises the step of: backing up first environmental status configuration at the time of power-off into the status back-up means; comparing the first environmental status configuration at the time of power-off backed up by the status back-up means with the second environmental status configuration when the power in turned on; and permitting the use the apparatus by a user when the first environmental status configuration is identical to the second environmental status configuration. The first environmental status configuration may include information derived by error detection process to the data pressured in the memory, connection status information of external memories or I/O port information.

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not to be considered as limiting the present invention.

Further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to thos skill d in the art form this detailed description.

Brief Description of the Drawings

Figs. 1A, 1B and 1C show a configuration of one embodiment of the present invention;

Fig. 1D shows the constructive relationship betw en Figs. 1A, 1B and 1C;
Fig. 2 shows a flow chart of an operation of the embodiment,
Fig. 3A, 3B, 3C and 3D show flow charts of a data back-up/restore system of the embodiment,
Fig. 4A, 4B, 4C and 4D show flow charts of the data back-up/restore system of the embodiment,
Fig. 5A and 5B show flow charts of the data back-up/restore system of the embodiment, and
Fig. 6 shows a conceptual view of the back-up to a back-up memory.

Description of the Preferred Embodiments

One embodiment of the present invention is now explained with reference to Figs. 1 to 6.

Figs. 1A, 1B and 1C show a configuration of an information processing apparatus of the present invention. The information processing apparatus comprises a CPU 10 which is control means, a CPU clock 20 for clocking the CPU 10 a main memory 30 for storing programs and data, a VRAM 40 for storing image data and permitting high speed access, a back-up memory 50 which preserves data when a system power is turned off, an input/output device 60 for controlling input/output, an auxiliary memory 70 for storing data and a power supply 80 for supplying powers to the respective units from a home power line or a battery. The CPU clock 20 includes a CPU clock supply 21 for generating a reference clock signal and a CPU clock-switch 22 for switching from the reference clock signal to a desired clock signal. The main memory 30 includes an OS (operating system) 31, a BIOS (basic input/output system) 32, a system management table 33 which manages connection status information of the auxiliary memory 70 and application programs 34. The BIOS 32 includes buzzer control means 32a power-off detection means 32b, status back-up means 32c, status restore means 32d and power control means 32e. The back-up memory 50 includes a memory sum correction value area 51 and a stock area 52. The input/output device 60 includes a keyboard 61, a keyboard interface 62, a display 63, a display controller 64, a back light 65 for illuminating the display 63, a buzzer 66 controlled by the buzzer control means 32a and a buzzer timer 67. The buzzer timer 67 is used to determine a frequency of the buzzer sound of the buzzer 66. The auxiliary memory 70 includes a floppy disk drive 71, a FDC (floppy disk controller) 72, a hard disk drive 73 and HDC (hard disk controller) 74. In the present embodiment, the CPU 10 gives instructions to the respective units through the bus line 90 along the processing of the BIOS 32 to attain the resume function. A small power is supplied to the main memory 30 and the back-up memory 50 after the power-off of the system power so that the data stored in those memories are preserved even after the power-off of th system power. Accordingly, the data which should be backed up at the power-off in order to attain the resume function in the back up memory 50 is the image data, and the data stored in the main memory is not backed up. The system environmental status configuration which is a feature of the present embodiment is also backed up to the back-up memory 50 at this stage.

Referring to a flow chart of Fig. 2, an operation from the power-off to the power-on and the information of the resumption of the data processing through the inform means is explained. When the power switch is tuned off (step 101) during the execution of the application program 34 (step 100), a power-off detection interruption signal 110 is generated and the control is shifted to a power-off process. The status of the CPU 10 is back up in the main memory 30 (step 111) and the content of the VRAM 40 is backed up in the back-up memory 50 (step 112). The content of the VRAM 40 is backed up in the back-up memory 50 in order to stop the supply of power to the VRAM 40 which comprises a high power consuming dual port memory. Then, the supply of power to the display 63, the back light 65, the VRAM 40 and the CPU 10 is stopped (step 113). Since the supply of power to the CPU 10 is stopped, the CPU 10 stops. The content backed up in the back-up memory 50 in the step 112 is preserved by the supply of power from the power supply 80. When the power is turned on (step 114), the CPU 10 starts the processing from the reset status (step 115) and the content backed up in the back-up memory 50 in the step 112 is restored (step 116). In order to inform the completion of the restore to the VRAM 40 to a user, the buzzer generates a short sound twice (step 117). It is not limited to the short sound of two times and it may be one time or more than two times, or a longer sound. The information may be done by displaying a message on the display 63 or flashing an LED lamp (not shown). The combination with the buzzer 66 enhances the effect. The status of the CPU 10 is restored so that the application program 34 is executed from the next instruction to the power-off detection interruption 110 (step 118). In this manner, the execution of the application program 34 is continued (step 120).

In the present embodiment, the inform means is active when the time of instruction to the processing apparatus and the time of operation of the processing apparatus are not simultaneous. Namely, at the time of completion of the data processing when th pow r is turned off or at th tim of start of the data processing when the power is turned

on, the buzzer sound is generated, the lamp is flashed, the display is flashed or the messag is displayed. By informing the status of the processing apparatus to the user, the user can exactly determine the timing to continue the operation. The effect of such inform means is great at various places when such means is installed small size portable equipments of the information processing apparatus.

The data back-up/restore system of the present embodiment is explained with reference to a flow chart of Fig. 3A, 3B, 3C and 3D. In the present system, it is assumed that the resume function can be selected by a dip switch or a software switch. The resume function is enabled or disabled by the software switch (step 200). If the resume function is enabled, an interruption request is issued when the power is turned off. When the power is turned off (step 202) during the execution of the application program 34 (step 201), whether the resume function has been enabled in the step 200 or not is determined (step 203). If the resume function has been enabled, the power-off detection interruption request 110 is issued and the control is shifted to the power-off process. If the resume function has been disabled in the step 200, the system is stopped. When the power-off detection interruption request 300 is issued, the status of the CPU 10, the status of the CPU clock, the value of the check sum which is the system environmental status configuration, the connection status of the auxiliary memory 70 and the status information of the I/O ports are backed up in the back-up memory 50 (step 310). The CPU 10 instructs to the CPU clock switch 22 to switch the clock of the CPU 10 to a maximum clock, 16MHz (step 320). Then, the content of the VRAM 40 is backed up in the back-up memory (step 330). After the back-up, the supply of powers to the display 63, the back light 65, the VRAM 40 and the CPU 10 is stopped (step 340). The user stops to use the personal computer under this condition. Thereafter, when the user turns on the power to use the personal computer (step 350), the reset sequence is executed as a system initialization process (step 360). The reset sequence is primarily executed for the VRAM 40 and not for the main memory 30 in which the data is preserved after the turn-off of the system power. The content of the VRAM 40 backed up in the back-up memory 50 in the step 330 is restored to the VRAM 40 (step 370). The value of the check sum, the connection status of the auxiliary memory 70 and th status information of the I/O port which were backed up in the back-up memory in the step 310 are read and they are compared with the current status (step 380). If they are not equal in the comparison, a message is displayed on the display 63 (step 390) and the system is stopped. The message may be "Cannot resume. Depress reset k y". The user is permitt d to use th system without the resume function by depressing the reset key. If they are equal in the step 380, the buzzer is activated to inform to the user that the user can use the personal computer (step 400). Substantially simultaneously with the buzzer alarm, the CPU clock speed and the status of the CPU 10 are restored from the back-up memory 50 (steps 410 and 420). The power-off detection interruption sequence 300 is thus completed and the application program 34 is executed in a continuous manner (step 210).

The back-up of the system environmental status configuration information which is the feature of the present embodiment is now explained with reference to Figs. 4A and 4B which show a flow chart of the step 310. A stack is set in the stack area 52 of the back-up memory 50 (step 311). Th speed of the CPU 10 and the status information of the CPU clock are stored in the stock area 52 (step 312). Flags which indicate the connection status of the devices including the floppy disk drive 71, the hard disk drive 73 and the RAM board are read from the system management table 33 of the main memory 30 and they are stored in the stack area 51 (step 313). Those flags have been set in th system management table 33 at the time of previous power-on of the system power. Similarly, the status information of the I/O port is read and stored in the stack area 52 (step 314). The memory sum correction value area 51 of the back-up memory 50 is initialized to "O" (step 315). The sum of the contents of the main memory 30 and the VRAM 40 produced by the check sum, which is one of error detection method, is stored in the stack area 52 (steps 316 and 317). Specifically, the contents of address 0 and even addresses of the memory are sequentially added. Similarly, the contents of address 1 and odd addresses are sequentially added. Low order one byte of each of the sums is stored in the stack area 52. A complement of the sum is stored in the memory sum correction valve area 51 (step 318). The reason for using the complement of the sum is for the comparisons of the system environment comparison information at the next power-on of the system power.

The back-up operation of the system environmental status configuration to the back-up memory 50 is summarized in Fig. 6. Complements of the sums of the odd address and the even addr sses are backed up in the memory sum correction value area 51. The flagindicative of the connection status of the auxiliary memory 70 backed up in the system manag ment table 33 and the status information of the I/O port are backed up in the stock area 52. Th image data stor d in the VRAM 40 is backed up in the back-up memory 50.

The restoring process of the system environmental status configuration which is executed after the power-on of the system power is explained with refer nce to Figs. 5A and 5B which show a flow chart of the step 370 and 380. The sum of the contents of odd address in the main memory 30 and contents of the even address in the main memory into the odd address sum and the even address sum, are calculated. The low order one byte of each of the sums is read. The complement data stored in the memory sum connection value area 51 of the back-up memory 50 is read and the complement data is added to the sum (step 371). If the content of the main memory 30 has not been destroyed from the system power-off to the next system power-on, the sum calculated in the step 316 at the time of system power-off and the sum in the step 371 are equal. Accordingly, if the content of the main memory 30 is correct, the addition of the complement data in the step 316 and the sum in the step 371 produces a sum "O". Similar calculation is mode for the image data of the VRAM 40 backed up in the back-up memory 50 (step 372) to determine whether the sum is "O" or not (step 381). Then, the status information of the I/O port is read and it is compared with the status information of the I/O port at the time of system power-off which is stored in the stack area 52 (steps 382 and 383). The devices such as the floppy disk drive 71, the hard disk drive 73 and the RAM board are actually operated to check the connection status (step 384). The result of the check is compared with the data relating to flag indicative of the connection status of the devices which is stored in the stock area 52(step 385). If the system environment is same that at the time of power-off through the comparison with the system environmental status configuration in the steps 381 to 385, the buzzer is activated to inform to the user that the system can be used (step 400). If they are not equal in the comparison, a message is displayed (step 390) and the system is stopped. The user is permitted to use the personal computer without using the resume function by depressing the reset key.

In the data back-up/restore system of the information processing apparatus of the present invention, the system environmental status configuration at the system power-off and the system environmental status configuration at the subsequent system power-on are computed to determine any change in the system status from the system power-off to the subsequent system power-on. By such determination, the user can exactly grasp the system status and can continuously use the information processing apparatus only when the system status has not changed.

From the invention thus described, it will b obvious that the invention may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Claims

1. An information processing apparatus comprising: memory means connected to control means through a bus line;

   status back-up means for backing up th status of said control means and the content of said memory means at the time of power-off;

   status restore means for restoring the status backed up in said status back-up means at the time of power-on to resume the data processing; and

   inform means for informing the termination of the data restoring processing.

2. A data back-up/restore system of an information processing apparatus comprising

   memory means connected to control means through a bus line; status back-up means for backing up the status of said control means and the content of said memory means at the time of power-off; and

   status restore means for restoring the status backed up by said status back-up means at the time of power-on to resume the data processing;

   said system comprising the steps of:

   backing up (first environmental status) configuration at the time of power-off by said status back-up means;

   comparing the first environmental status configuration at the time of power-off backed up by said status back-up means with a second environmental status configuration when the power in turned on; and

   permitting the use of the apparatus by a user when the first environmental status configuration is identical to the second environmental status configuration.

3. A data back-up/restore system of the information processing apparatus according to Claim 2, wherein the first environmental status configuration is error detection processing information for the data backed up by said status back-up means.

4. A data back-up/restore system of the information processing apparatus according to Claim 2 wherein the first environmental status configuration is device connection status information.

5. A data back-up/restore system of the information processing apparatus according to Claim 2 wherein the first environmental status configuration includes I/O port status information.

6. A data back-up/restor system of the information processing apparatus according to Claim 2 wherein a processing speed of said control means from the back-up by said status back-up means to the restore by said status restore means is changed to a high speed irrespectively of a current speed.

Fig. 1A

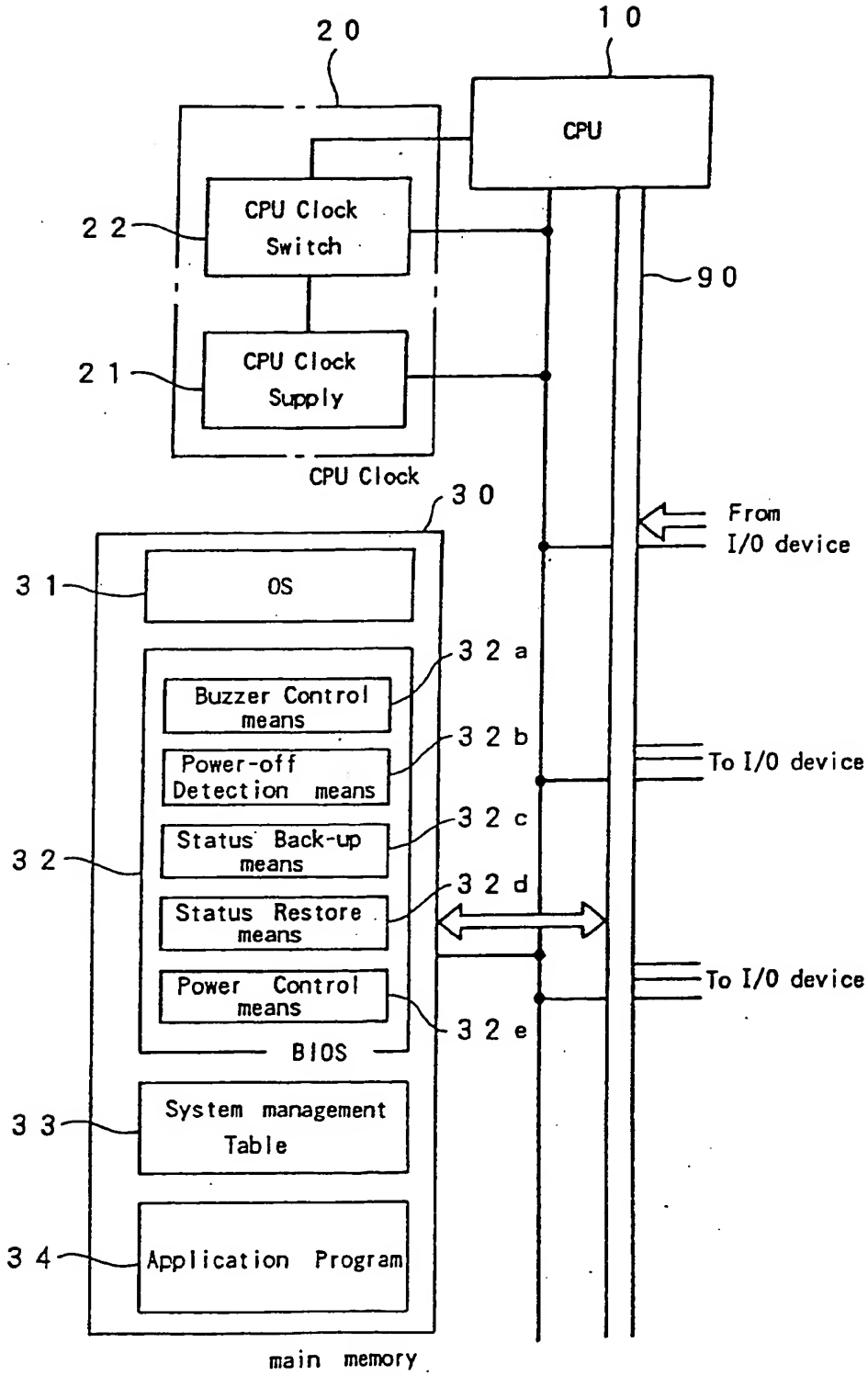

20
10
CPU
CPU Clock Switch
22
90
CPU Clock Supply
21
CPU Clock
30
From I/O device
31
OS
32a
Buzzer Control means
32b
Power-off Detection means
To I/O device
32c
Status Back-up means
32
32d
Status Restore means
Power Control means
To I/O device
32e
BIOS
System management Table
33
Application Program
34
main memory

Fig. 1B

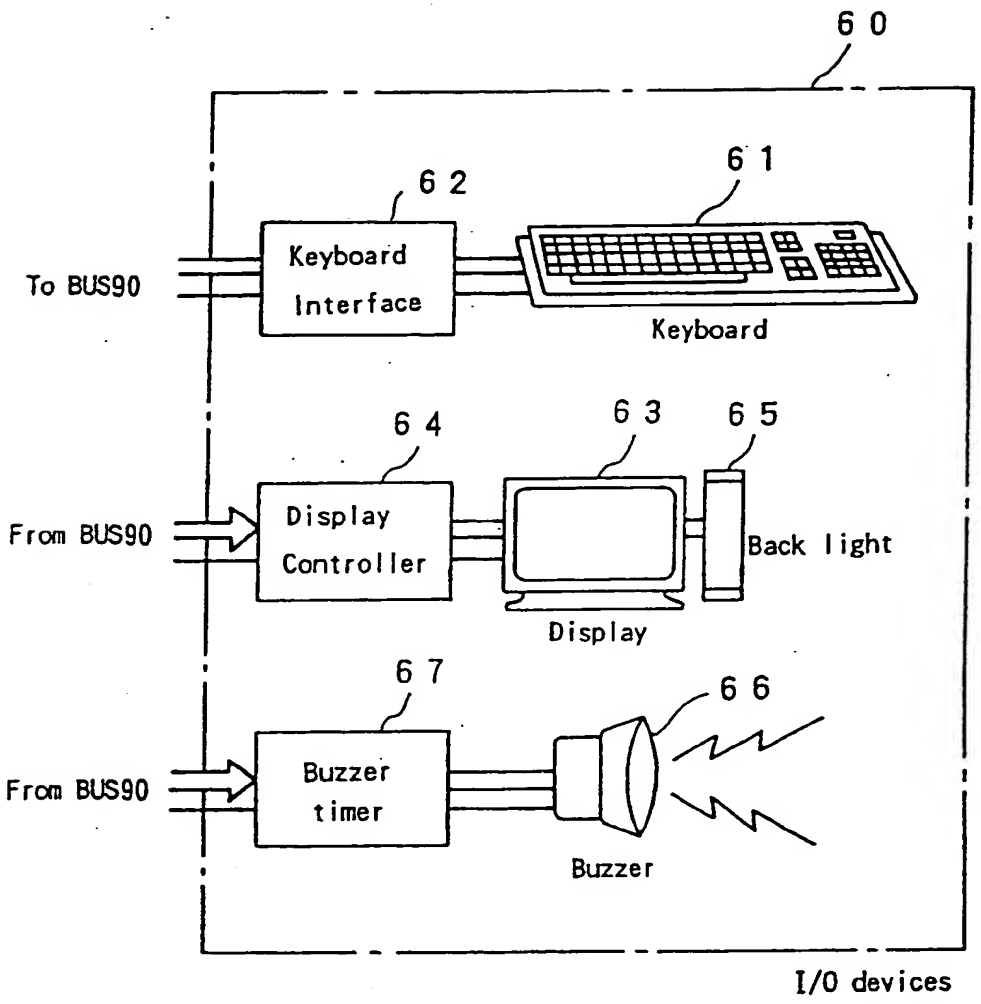

60
62
61
To BUS90
Keyboard Interface
Keyboard
64
63
65
From BUS90
Display Controller
Back light
Display
67
66
From BUS90
Buzzer timer
Buzzer
I/O devices

Fig. 1C

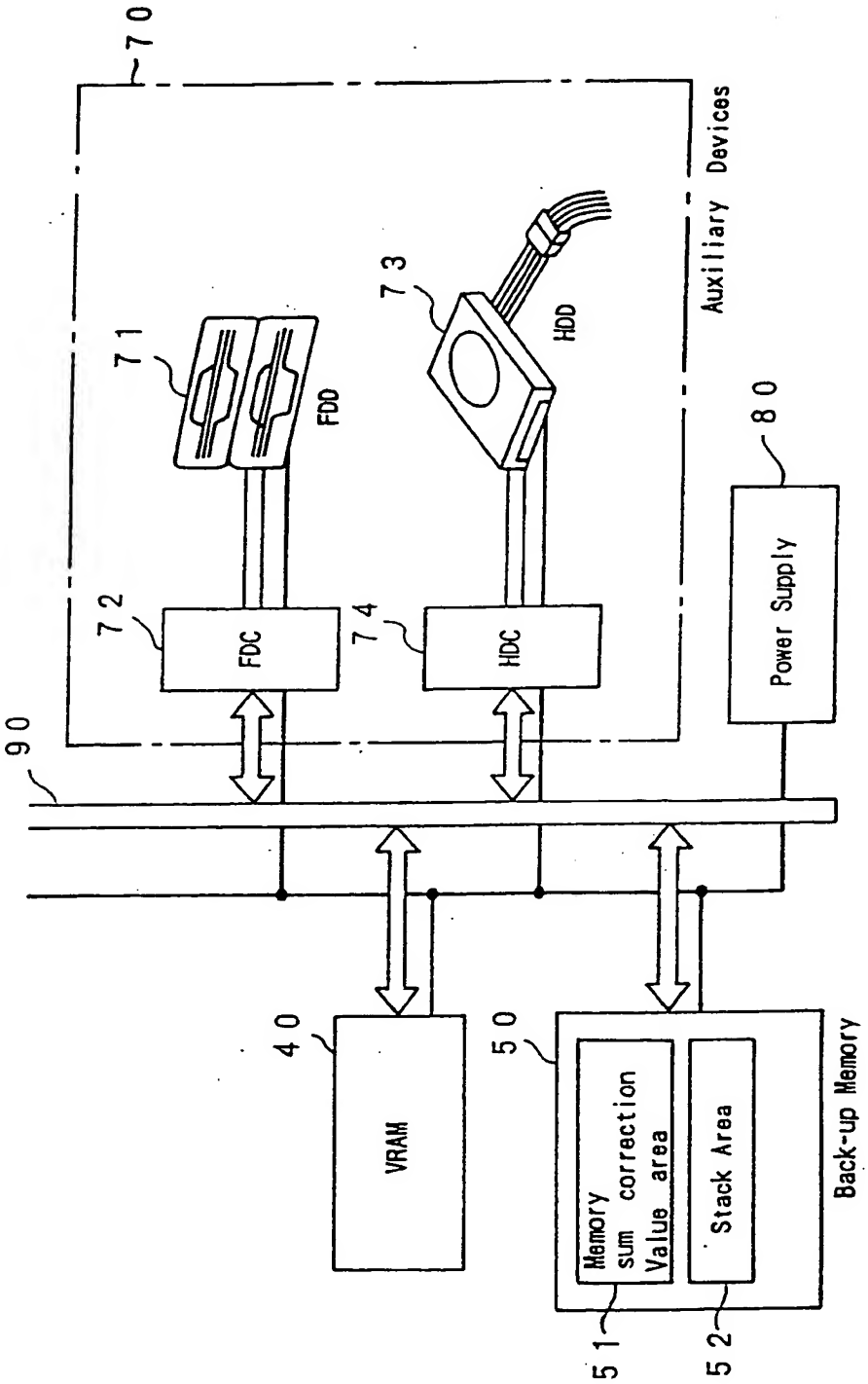

70
Auxiliary Devices
71
FDD
73
HDD
80
Power Supply
72
FDC
74
HDC
90
40
VRAM
50
Memory sum correction Value area
Stack Area
Back-up Memory
51
52

Fig. 1D

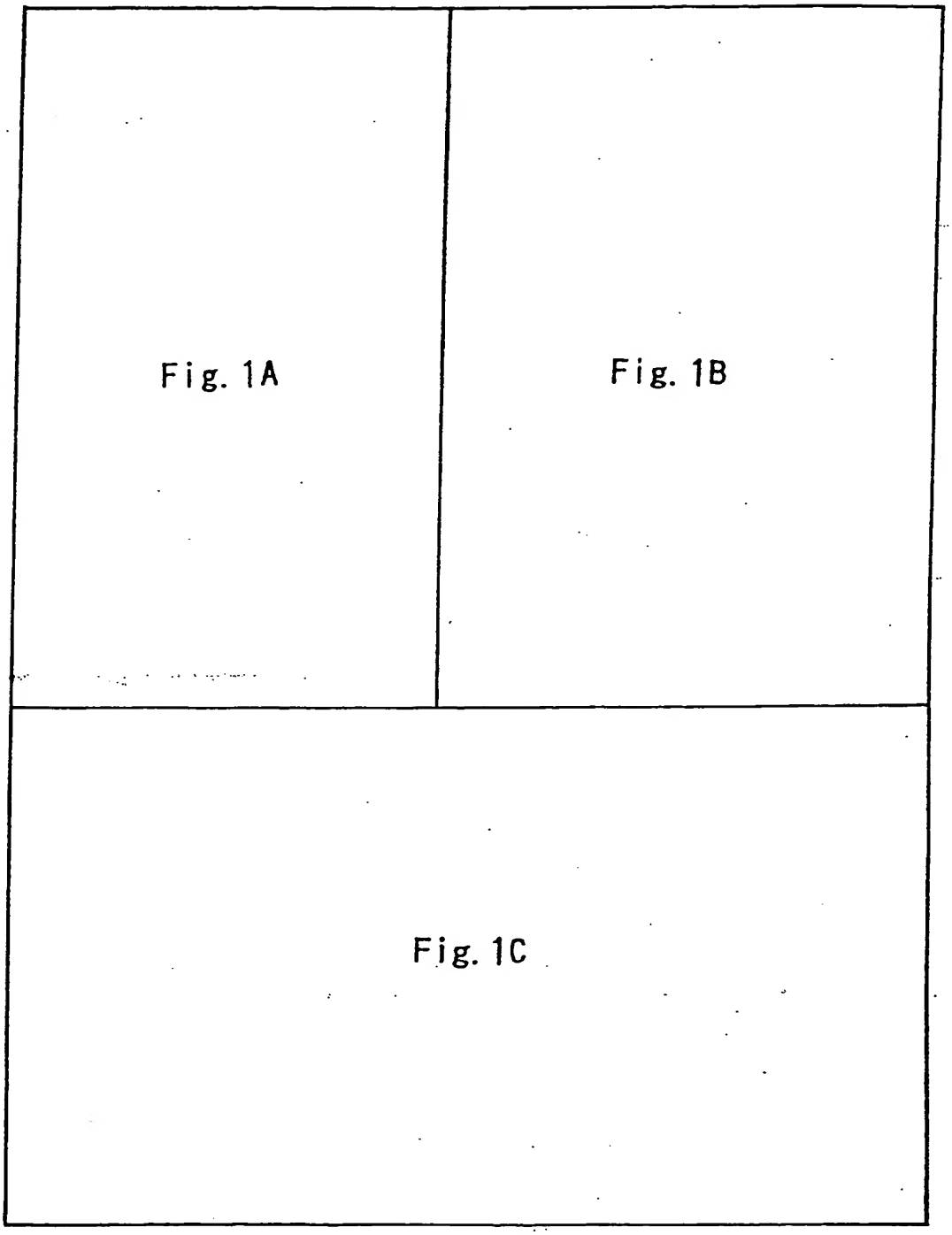


Fig. 2

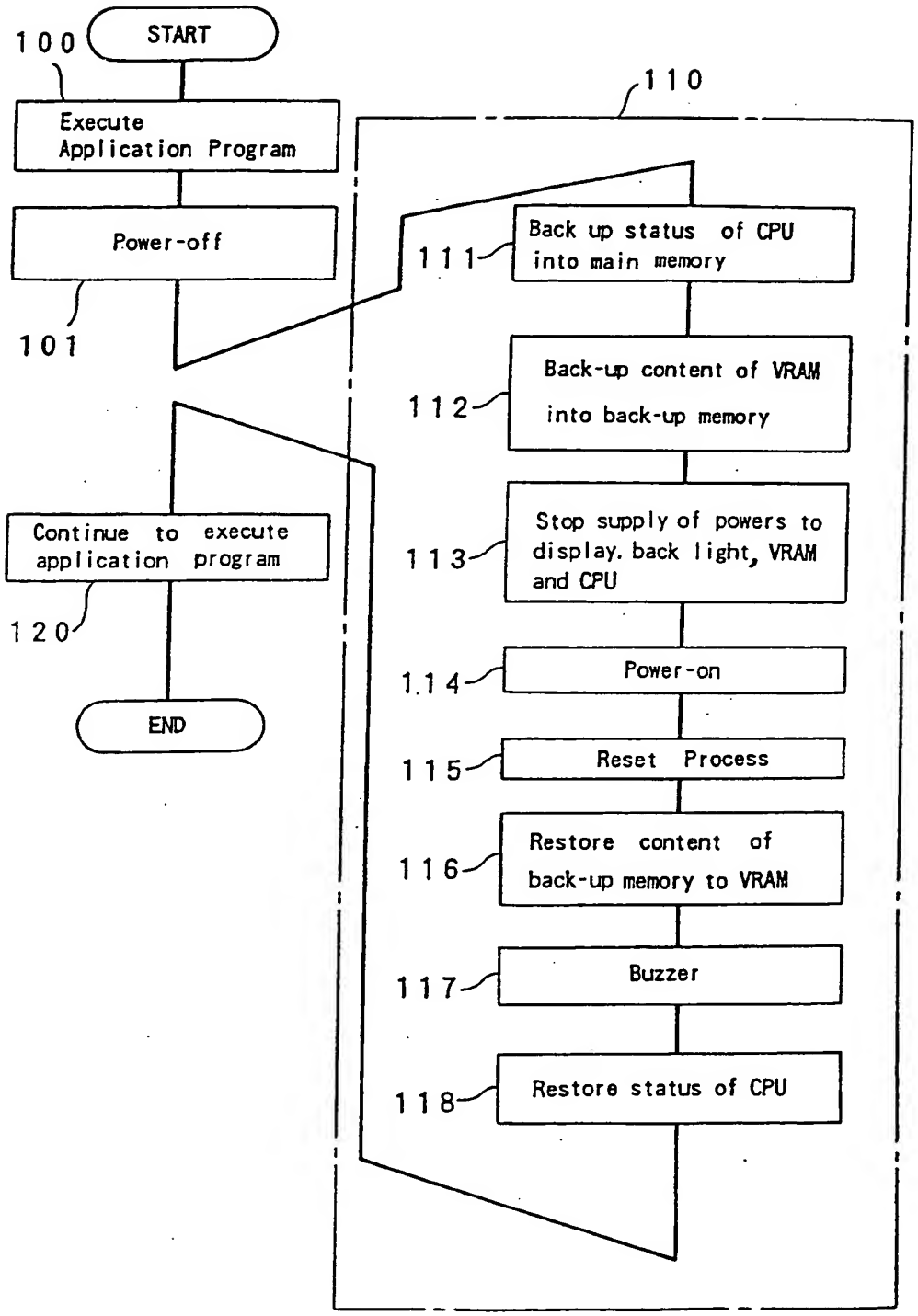

100
START
Execute Application Program
Power-off
101
110
111
Back up status of CPU into main memory
112
Back-up content of VRAM into back-up memory
113
Stop supply of powers to display. back light, VRAM and CPU
114
Power-on
115
Reset Process
116
Restore content of back-up memory to VRAM
117
Buzzer
118
Restore status of CPU
Continue to execute application program
120
END

Fig. 3A

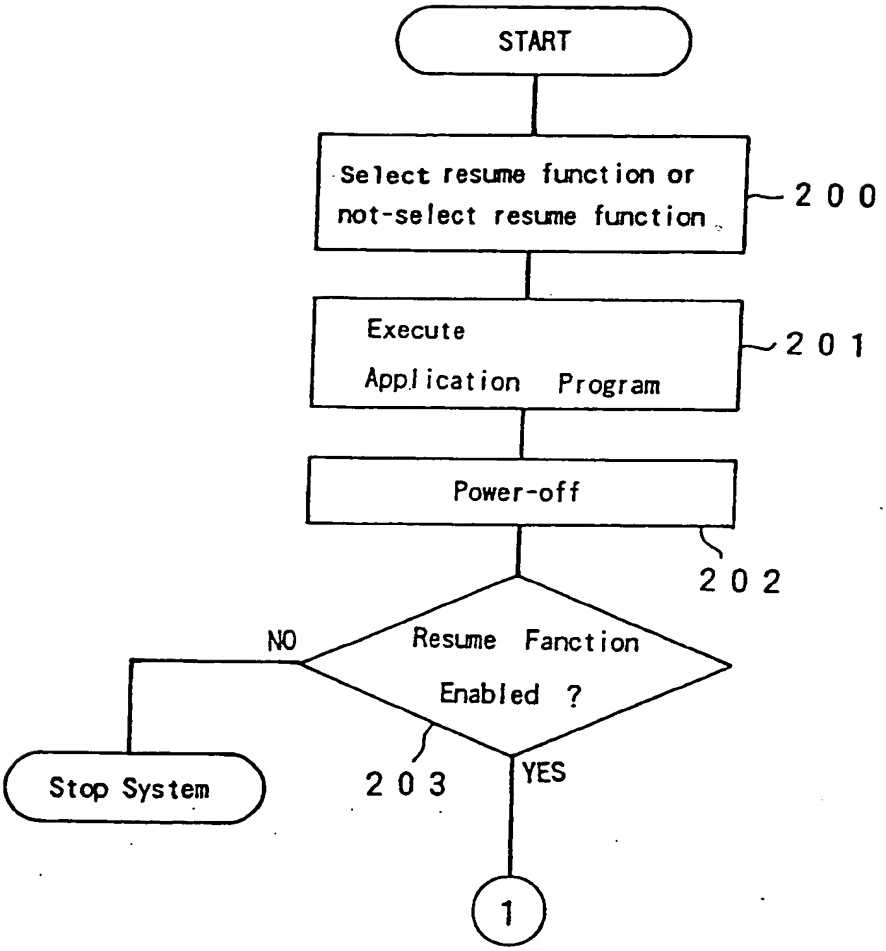

START
Select resume function or not-select resume function
200
Execute Application Program
201
Power-off
202
NO
Resume Fanction Enabled ?
203
YES
Stop System
1

Fig. 3B

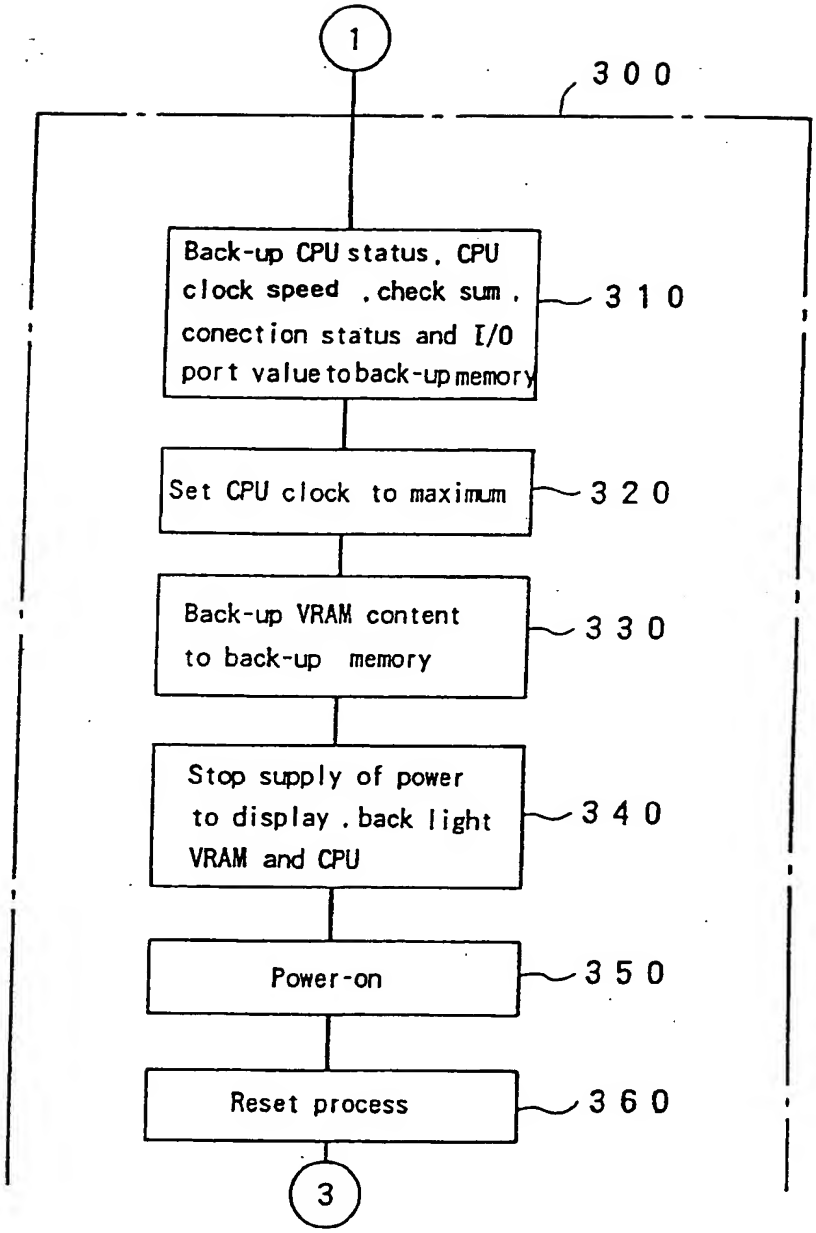

1
300
Back-up CPU status, CPU clock speed, check sum, conection status and I/O port value to back-up memory
310
Set CPU clock to maximum
320
Back-up VRAM content to back-up memory
330
Stop supply of power to display, back light VRAM and CPU
340
Power-on
350
Reset process
360
3

Fig. 3C

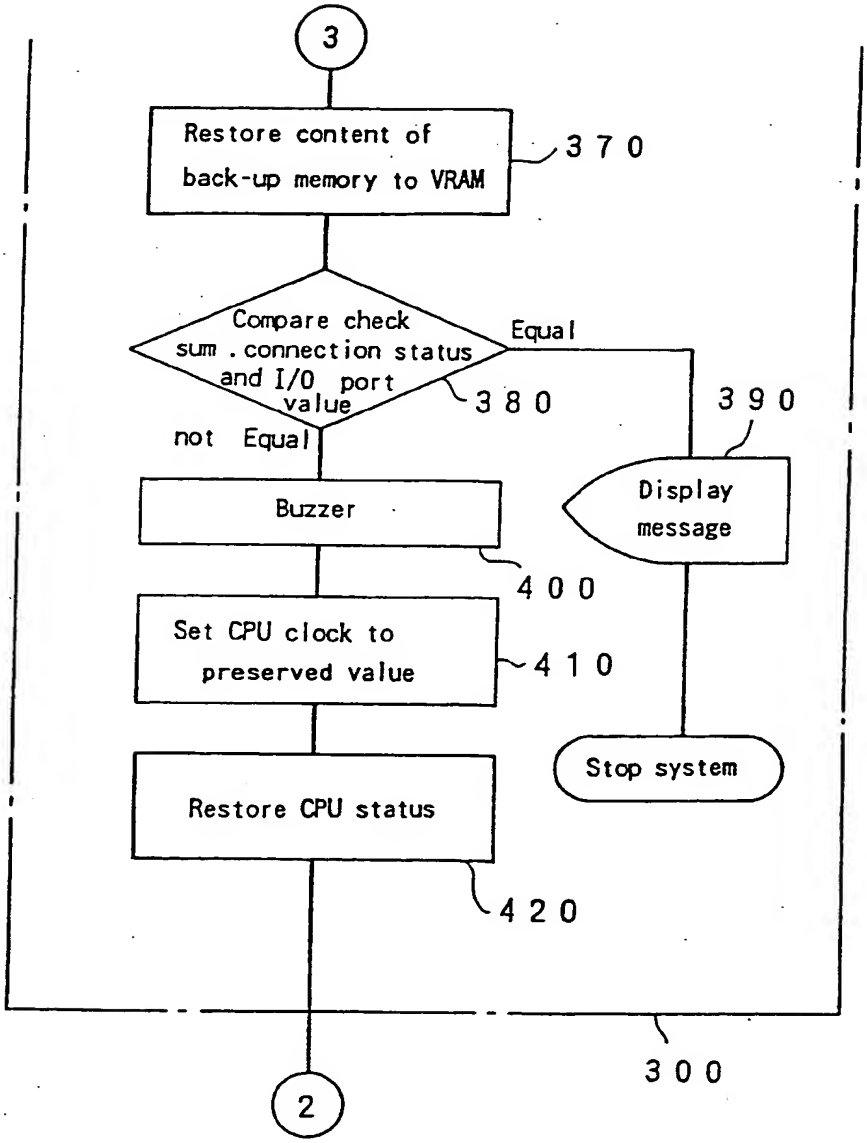

3
Restore content of back-up memory to VRAM
370
Compare check sum . connection status and I/O port value
380
Equal
390
not Equal
Buzzer
400
Display message
Set CPU clock to preserved value
410
Stop system
Restore CPU status
420
300
2

Fig. 3D

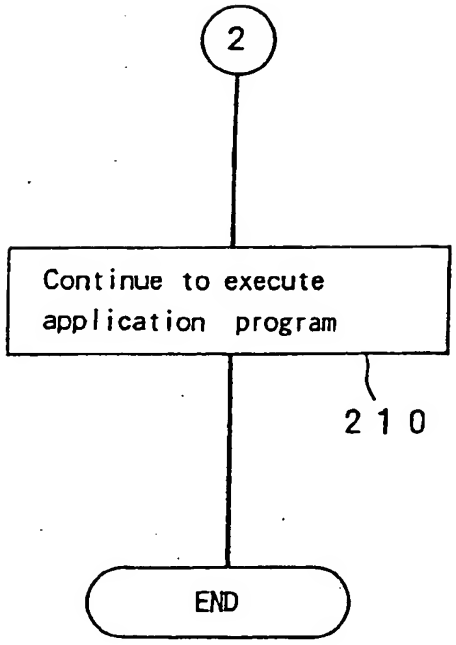


Fig. 4A

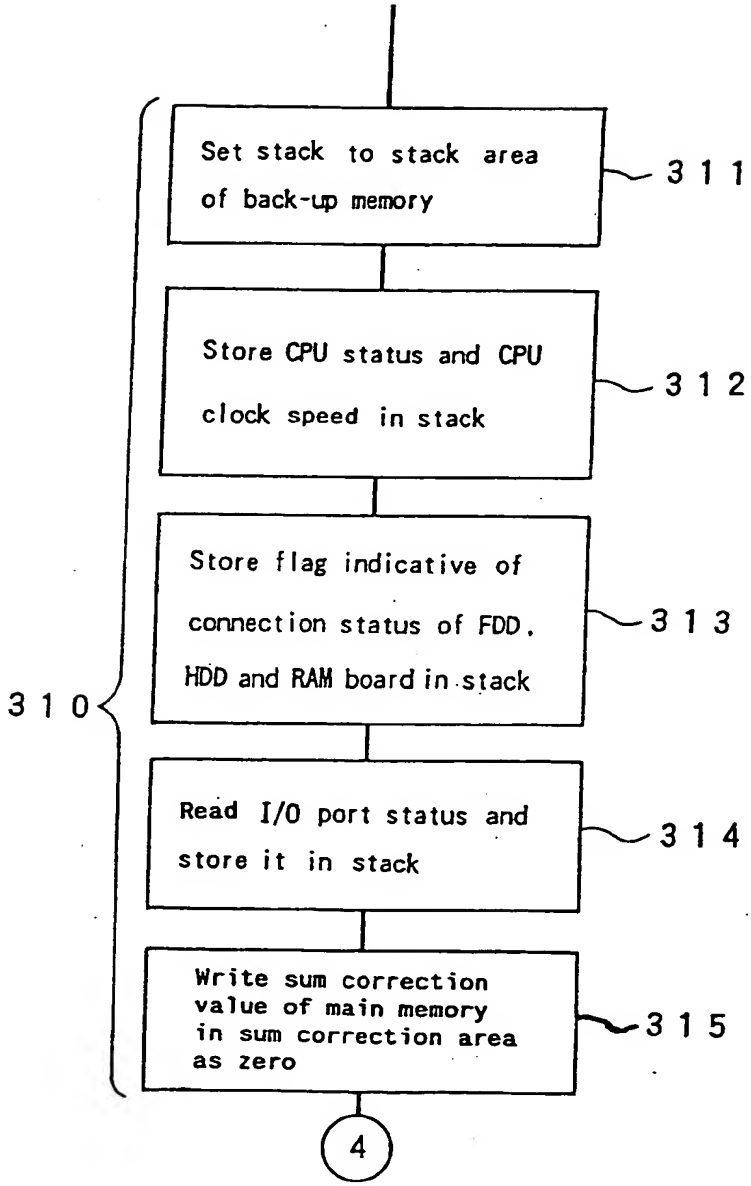

Set stack to stack area of back-up memory
311
Store CPU status and CPU clock speed in stack
312
Store flag indicative of connection status of FDD, HDD and RAM board in stack
313
310
Read I/O port status and store it in stack
314
Write sum correction value of main memory in sum correction area as zero
315
4

Fig. 4B

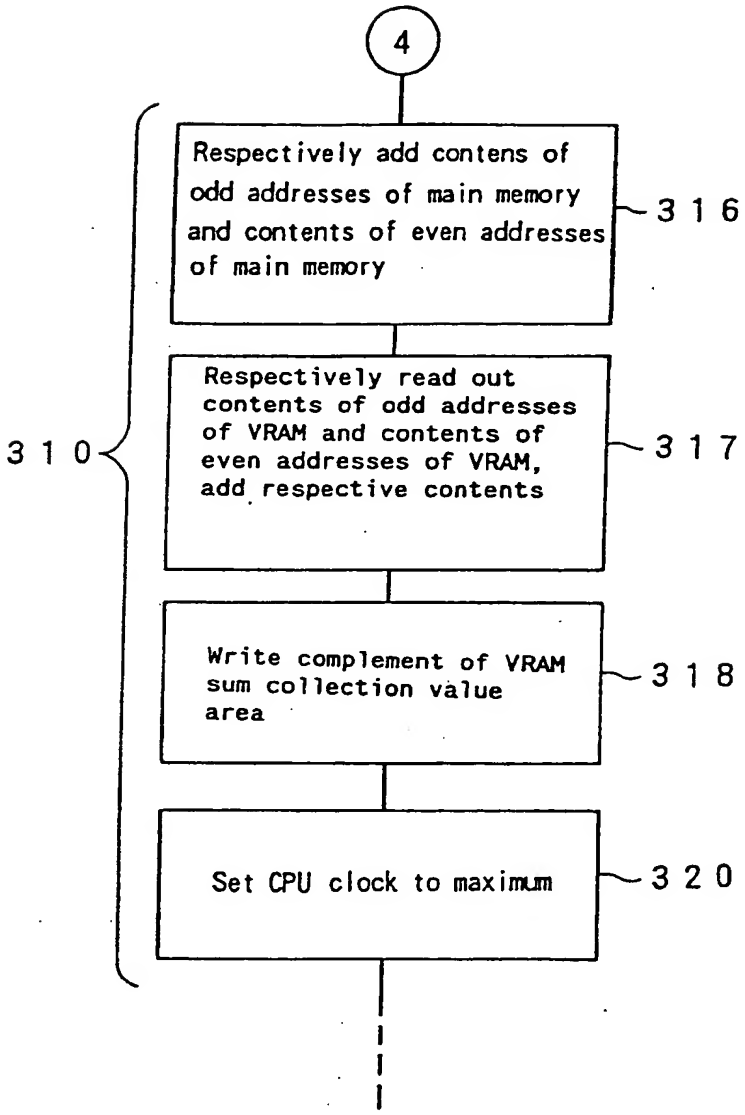

4
Respectively add contens of odd addresses of main memory and contents of even addresses of main memory
316
Respectively read out contents of odd addresses of VRAM and contents of even addresses of VRAM, add respective contents
317
310
Write complement of VRAM sum collection value area
318
Set CPU clock to maximum
320

Fig. 5A

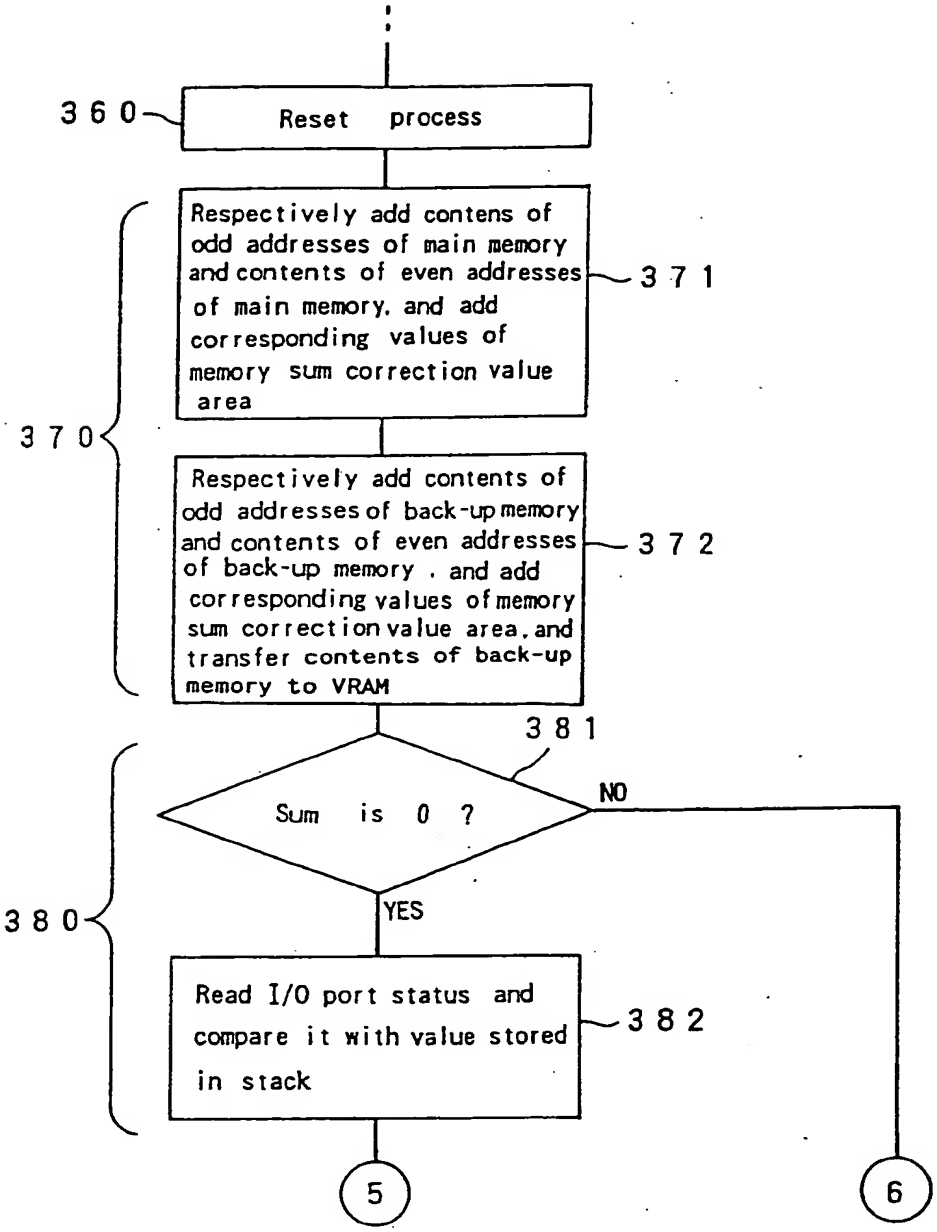

360
Reset process
370
Respectively add contens of odd addresses of main memory and contents of even addresses of main memory, and add corresponding values of memory sum correction value area
371
Respectively add contents of odd addresses of back-up memory and contents of even addresses of back-up memory , and add corresponding values of memory sum correction value area, and transfer contents of back-up memory to VRAM
372
381
Sum is 0 ?
NO
YES
380
Read I/O port status and compare it with value stored in stack
382
5
6

Fig. 5B

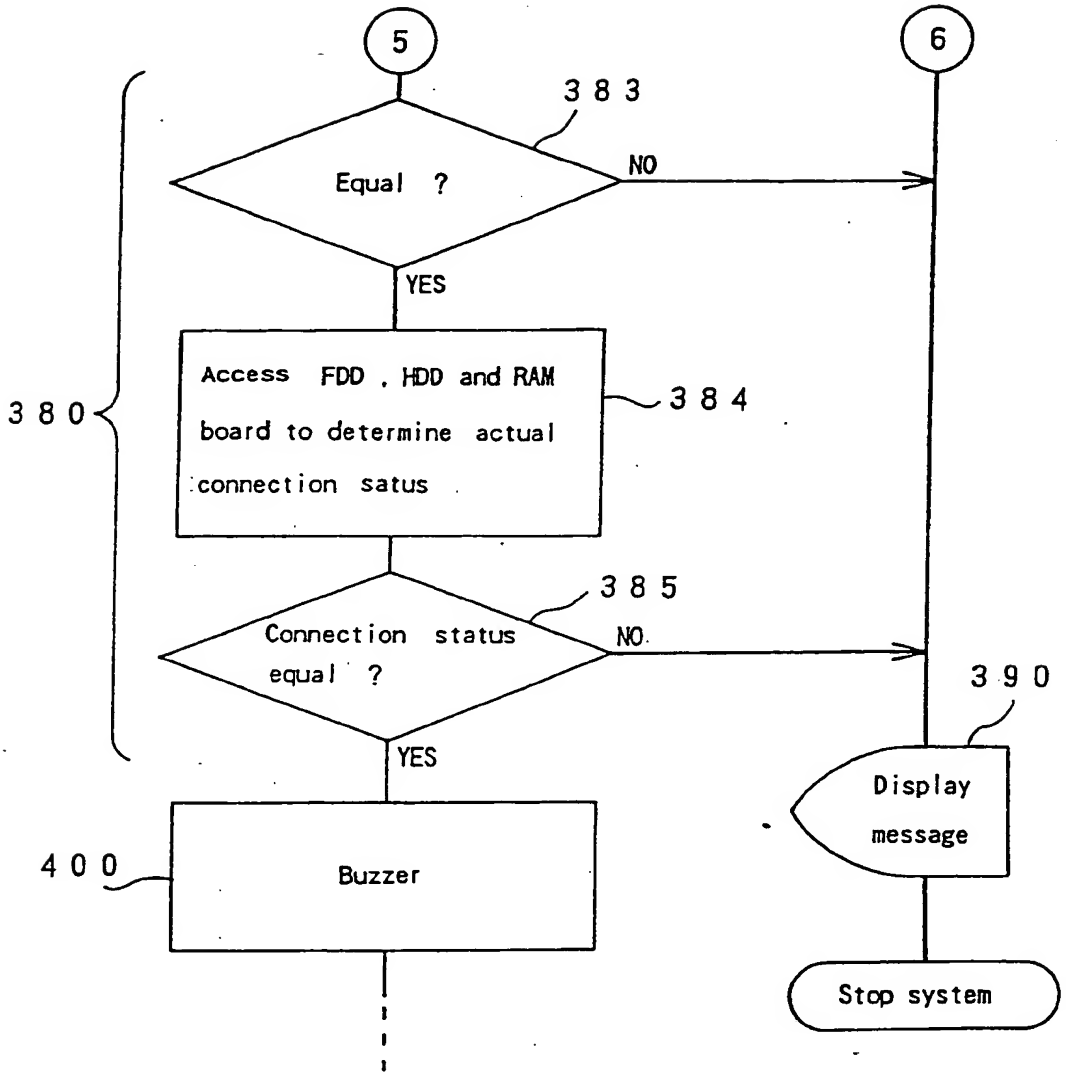
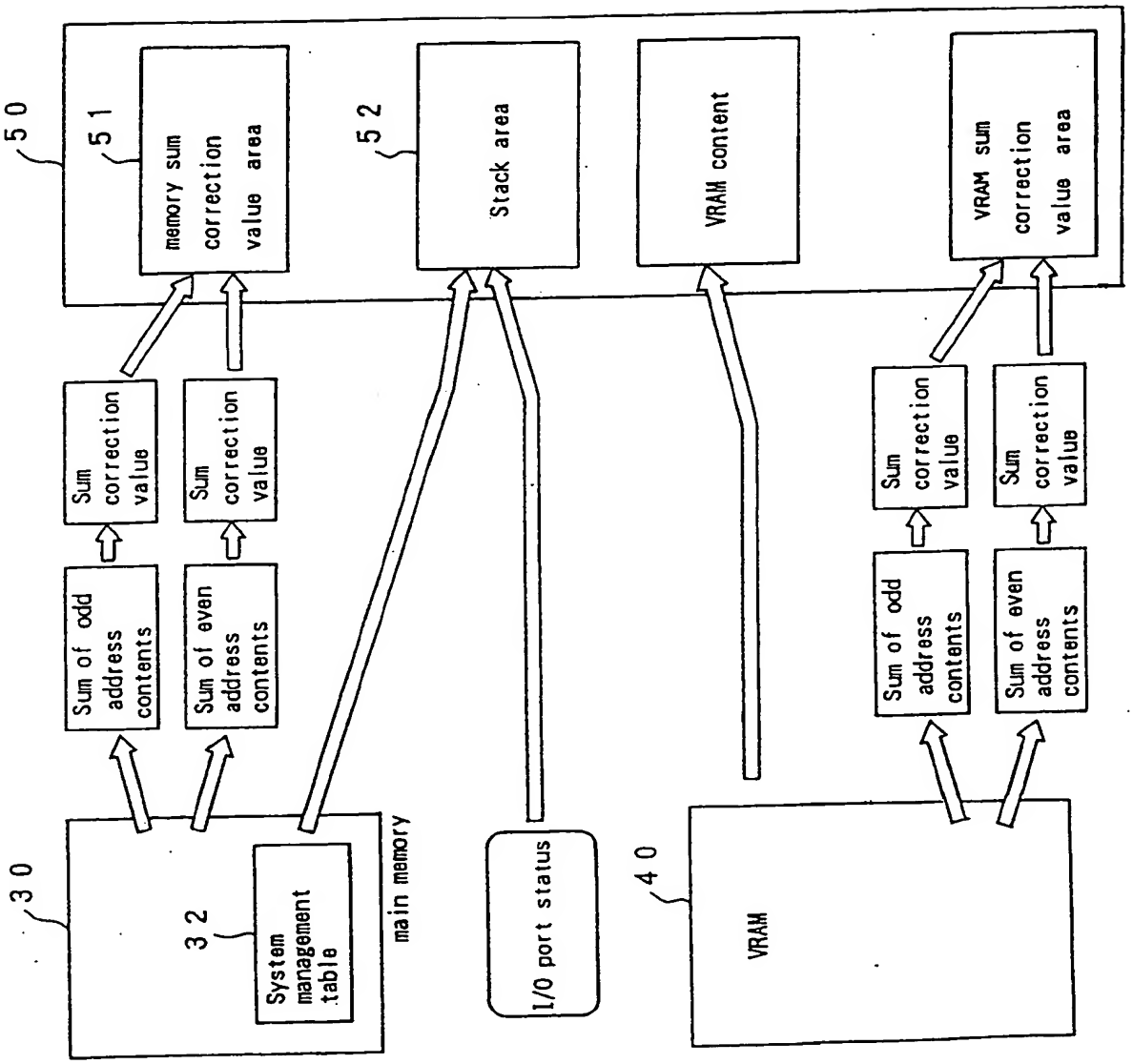

5
6
383
Equal ?
NO
YES
Access FDD , HDD and RAM board to determine actual connection satus
384
380
385
Connection status equal ?
NO
390
YES
Display message
400
Buzzer
Stop system

Fig. 6


50
51
memory sum correction value area
52
Stack area
VRAM content
VRAM sum correction value area
Sum correction value
Sum correction value
Sum correction value
Sum correction value
Sum of odd address contents
Sum of even address contents
Sum of odd address contents
Sum of even address contents
30
32
System management table
main memory
I/O port status
40
VRAM